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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/695,756	10/24/2000	Thomas W. Voshell	500080.02	2589

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DORSEY & WHITNEY LLP
INTELLECTUAL PROPERTY DEPARTMENT
SUITE 3400
1420 FIFTH AVENUE
SEATTLE, WA 98101

EXAMINER	
LAMARRE, GUY J	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 10/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/695,756	VOSHELL	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *41-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *41-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

0. This office action is in response to Applicants' **Amendment**, filed on *09 July 2002*. The change of address, filed 5/29/02, has been entered.

0.1 Claims **41-67** remain pending.

0.2 The art rejections of record to Claims **41-67** stand maintained in response to Applicants' **Amendment**, filed on *09 July 2002*.

Response to Arguments

1. Applicants' arguments, filed on *09 July 2002*, have been fully considered but they are not persuasive. **Examiner** notes that the words: **"faulty** and **defective"** are equivalent.

REMARKS

2.0 In response to claims **41** and **45**, Applicants argue that **Tsukakoshi** does not disclose procedures comprising: comparing address means including compressed address format features, replacement or substitution or allocation means based on result of said comparison.

Examiner disagrees as such recitations are clearly disclosed in SUMMARY OF THE INVENTION or in col. 2 lines 35-50, e.g., " *The memory fault analysis apparatus of the present invention is provided with an algorithmic pattern generator which generates* ***address signals*** *for selecting a memory cell of a memory to be analyzed, and that has a redundancy circuit and generates data which is written to a selected memory cell; a* comparison means *performs read after data has been written to a selected memory cell by address signals and then compares the read data and data from an algorithmic pattern generator to determine whether or not it is in agreement. If it is not in* ***agreement a fault signal which indicates that the memory cell is faulty is generated****. An* ***address allocation means*** *receives address signals from an algorithmic pattern generator and performs address allocation for a fault analysis memory so that a plural number*

of memory cells of a memory under test (MUT) correspond based on a predetermined rule to a single memory cell of a fault analysis memory. The fault analysis memory writes fault information in to a memory cell corresponding to a memory cell of the memory under ***test which has the fault, when fault signals indicating the fault are sent from the comparison means****. According to the memory fault analysis apparatus of the present invention and having the configuration described above, the address allocation means performs address allocation, that is, address compression for the fault analysis memory so that a plural number of memory cells of the MUT correspond on the basis of a predetermined rule to one of the memory cells of the fault analysis memory, when at least one memory cell of the plural number of memory cells is faulty, there is the write of fault information to the memory cell corresponding to the fault analysis memory. By performing address compression, the size of the area necessary for the FAM becomes smaller than that required in the conventional apparatus and by this it is possible to reduce the judgment time for fault recovery."*

In other words, in contrast to applicant's allegations on page 3 last para., when memory cell is determined as defective, means is provided for substitution of address of said memory cell with a different address of non-faulty memory cell. Means is also provided, in col. 2 lines 35-50, for address compression, e.g., "***address compression*** *for the fault analysis memory so that a plural number of memory cells of the MUT correspond on the basis of a predetermined rule to one of the memory cells of the fault analysis memory, when at least* ***one memory cell*** *of the plural number of memory cells* ***is faulty****, there is the write of* ***fault information*** *to the memory cell corresponding to the fault analysis memory. By performing* ***address compression****, the* ***size of the area necessary for the FAM becomes smaller*** *than that required in the conventional apparatus and by this it is possible to reduce the judgment time for fault recovery."* Examiner

does not understand how applicant fails to see or realize that address compression necessarily involves comparing means for subsequent memory access.

2.1 In response to claims 42-**43, 46-48, 54-64**, Applicants also allege that the combination of **Tsukakoshi and Hoang** does not render the invention as claimed unpatentable because **Tsukakoshi** 's deficiencies are not cured by **Hoang.**

Examiner disagrees as **Tsukakoshi** and **Hoang** clearly disclose the limitations as claimed. Examiner maintains that these claims are not allowable in their present form.

2.2 In response to claims **44, 49-53, 65-67**, Applicants also allege, on page 8, 1st para., last sentence, that **Tsukakoshi** teaches logging defective memory locations as opposed to substitution of good memory for defective memory locations. Applicants are referred to **Tsukakoshi** for substitution or replacement of good memory for defective memory locations, e.g., "*FIG. 6 shows the MUT 50 and this MUT 50 has a memory cell array 51, a row redundancy circuit 52 and a column redundancy circuit 53. When the cell line of the memory cell array 51 for which the row address is 2X and the column address is 2Y is faulty and the cell row for which the row address is 2X* ***is replaced*** *with the redundancy cell row 52a of the row redundancy circuit 52, the cell row for which the row address is 2X+1 is also* ***replaced*** *at the same time with the other redundancy cell row 52b of the row redundancy circuit 52, and when the cell column for which the column address is 2Y is replaced with the redundancy cell column 53a of the column redundancy circuit 53, the cell column for which the column address is 2Y+1 is also replaced at the same time with the other redundancy cell column 53b of the column redundancy circuit 53, then the number of rows and columns that are* ***replaced*** *at the same time is two each,*" in col. 1 line 9 and col. 3 line 33 et seq.

Claim Rejections - 35 USC ' 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3.1 Claims 44, 49-53, 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsukakoshi** (US Patent No. 5,363,382; Nov. 13, 1991) in view of **Meaden** (US Patent No. 4,642,793; March 19, 1984).

As per Claims 44, 49-53, 65-67, Tsukakoshi substantially discloses the procedure for the claimed method of claim 42. **Not specifically described** in detail in **Tsukakoshi** is the step whereby calculating a value from the memory address comprises dividing the value represented by the memory address by a prime number or use of hashing code or function.

However such memory address generation approach is well known in data compression. For example, **Meaden,** in an analogous art, discloses algorithms in "*Many-to-one mapping hash address generator*" wherein such techniques are described. {See **Meaden,** Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Tsukakoshi** by including therein address generation means via prime numbers or hashing code or function as taught by **Meaden,** because such modification would provide the procedure disclosed in **Tsukakoshi** with a technique whereby "***The indicator R is also applied to the address input of a random access memory 37 having four locations, each of which contains a prime number in the range 3-251. The contents of the addressed location of the memory 37 supply the hashing key K for the hash coding circuit 30.***" {See **Meaden, col.** 3 line 27 et seq.}

3.1.1 Claims 44, 49-53, 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsukakoshi** (US Patent No. 5,363,382; Nov. 13, 1991) in view of **Matsuda** (US Patent No. 5,659,737; August 1, 1995).

As per Claims 44, 49-53, 65-67, Tsukakoshi substantially discloses the procedure for the claimed method of claim 42. **Not specifically described** in detail in **Tsukakoshi** is the step whereby calculating a value from the memory address comprises dividing the value represented by the memory address by a prime number or use of hashing code or function.

However such memory address generation approach is well known in data compression. For example, **Matsuda,** in an analogous art, discloses algorithms in "*Methods and apparatus for data compression that preserves order by using failure greater than and failure less than tokens*" wherein such techniques are described. {See **Matsuda,** Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Tsukakoshi** by including therein address generation means via prime numbers or hashing code or function as taught by **Matsuda,** because such modification would provide the procedure disclosed in **Tsukakoshi** with a technique whereby "***FIG. 2 conceptually illustrates a mapping of predictive substrings, PS, from the character string 105 into the hash table 110. As shown by the lines and arrows in FIG. 2, for each predictive substring (PS), a hash index, specified by a hash function, maps the (PS) into an entry in the hash table 110. For the example shown in FIG. 2, the predictive substring (PS.sub.i) containing the characters "ABC" maps into a hash table entry for storage of the successive character "D." Similarly, for the additional substrings (PS.sub.i+1, PS.sub.i+2, and PS.sub.i+3), each predictive substring maps into the hash table 110. These examples assume that the natural language indications properly predict the successive character. The order of the characters in hash table 110 is merely exemplary, and the actual storage of characters is based on the hash function. Any hash based predictive function may be used in conjunction with the present***

invention to map the predictive substrings into the entries of hash table 110. In one embodiment, a remainder of division technique is used. The remainder of division technique is defined by the function h(key)=key MOD M where the devisor M determines the effective size of the hash table and is a prime number. The key is defined as the predictive substring. The remainder of division hash function works well when the block size is relatively small, such as when the block size is 3." {See **Matsuda, col. 2** line 56 et seq.}

3.1.2 Claims 44, 49-53, 65-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tsukakoshi** (US Patent No. 5,363,382; Nov. 13, 1991) in view of **NN8806199** (Improved Hash and Index Searching Techniques for Computers Using a Cache And/Or Virtual Memory; IBM Technical Disclosure Bulletin, June 1988, US; VOLUME NUMBER: 31, PAGE NUMBER: 199 – 202, hereinafter **IBM Tech**).

As per Claims 44, 49-53, 65-67, Tsukakoshi substantially discloses the procedure for the claimed method of claim 42. **Not specifically described** in detail in **Tsukakoshi** is the step whereby calculating a value from the memory address comprises dividing the value represented by the memory address by a prime number or use of hashing code or function.

However such memory address generation approach is well known in data compression. For example, **IBM Tech,** in an analogous art, discloses algorithms wherein such techniques are described. {See **IBM Tech,** Id., Abstract.} **Therefore**, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of **Tsukakoshi** by including therein address generation means via prime numbers or hashing code or function as taught by **IBM Tech,** because such modification would provide the procedure disclosed in **Tsukakoshi** with a technique whereby ***"many subsets of the chained blocks are arranged so that they are contained in the same memory segment and their relative order is maintained. The standard index table contains an entry for each block comprising the array. The modified indexing table contains an entry for each memory segment that contains a logically contiguous subset of the chained blocks. In addition, each table entry contains a***

count of the number of blocks mapped by the entry, that is, the number of blocks contained within the memory segment indicated by the entry. If many blocks fit within a single memory segment, each entry in the indexing table may indicate several blocks instead of just one. This table is more compact than a general index that pointed to each block and therefore will cause less page and cache faults, in addition to occupying less memory. The modified indexing structure is shown in Fig. 3. The same set of blocks as used in Fig. 2 are modified into a smaller indexing table." {See **IBM Tech,** last 10 lines.}

Conclusion

4.0 THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

4.1 The prior art made of record and relied upon is considered to applicant's disclosure. The references cited in Form PTO-892 are for the Applicant's review and comments.

4.2 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to:

(703) 746-7238, (for After-Final communications),

(703) 746-7239, (for formal communications intended for entry),

(703) 746-7240 (for informal or draft communications, please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached on (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Guy J. Lamarre, P.E.

Patent Examiner

9/24/02

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100